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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,201	06/06/2001	Sam Heidari	VELCP015	1732
28436	7590	11/30/2004	EXAMINER	
IP CREATORS P. O. BOX 2789 CUPERTINO, CA 95015			TRAN, KHANH C	
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			2631	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/876,201

Applicant(s)

HEIDARI ET AL.

Examiner

Khanh Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8 is/are allowed.
- 6) ☒ Claim(s) 1-5, 10, 12-13, 17 and 18 is/are rejected.
- 7) ☒ Claim(s) 6, 7, 9, 11, 14-16, 19 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/26/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The Preliminary Amendment filed on 03/14/2003 has been entered. Claims 1-20 are pending in this Office action.

Claim Objections

2. Claim 9 is objected to because of the following informalities: in line 1, "The apparatus of Claim 1" should be changed to -- The method of claim 8 --. Appropriate correction is required.

Specification

3. The disclosure is objected to because of the following informalities: on page 9, line 7, "decimator 124" should be changed to -- variable TEQ 124.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 1-5, 10, 12-13, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. U.S. Patent 6,754,261 B1 in view of Uesugi et al. U.S. Patent 5,563,911.

Regarding claim 1, Liu et al. invention is directed to method for determining a sampling time for a time domain equalizer (TEQ) in the DMT transceiver as shown in figure 8 for reducing intersymbol interference (ISI) in a receiving communication channel. Figure 7 illustrates an exemplary ADSL modem including a DMT transceiver 704 as also shown in figure 8. In view of that, the DMT transceiver in figure 8 corresponds to the claimed apparatus for suppressing intersymbol interference in the preamble.

In column 24 lines 35-67, figure 20 shows the relevant logic blocks of the block 831 shown in figure 8. The block 831 includes an analog filter 2002, analog-to-digital converter (ADC) 2004, and digital filter 2006. The A/D converter typically oversamples the received signal at a predetermined multiple N times the Nyquist rate. The digital filter 2006 filters the over-sampled sequence received from the ADC 2004, and performs a decimation function to provide a sequence of samples to the TEQ. Liu et al. further teaches that the digital filter may output every Nth filtered sample to the TEQ 832. The over sampled sequence includes N separate Nyquist rate sequences, each consisting of every Nth filtered sample starting from different delay within the oversampled sequence. In view of the foregoing teachings, the digital filter 2006 performs function as a decimator to output one of N separate Nyquist rate sequences to

the TEQ 832. Hence, the digital filter 2006 corresponds to the claimed "*means for adjusting the sampling rate*".

Liu et al. discloses a TEQ 832 as recited above, however, Liu et al does not teach the TEQ 832 as set forth in the claim.

Uesugi et al. discloses an equalizer for use in a data receiver, in which the number of required taps is reduced without impairing the effect of compensation of waveform distortion due to the components appearing after the main waveform component relative to time and that due to the components appearing before the main waveform component relative to time; see column 2, lines 46-67. The aforementioned phenomenon is called intersymbol interference as well known in the art of communications. Figure 4 illustrates an embodiment of the equalizer including a plurality of delay elements 2, a plurality of weighting elements 3 applied to an adder 4, a plurality of selector switches 7a to 7e disposed in line with the respective delay elements 2; see figure 3, lines 45-67. In operation, the selector switches disposed in line with the delay lines of the equalizer are utilized to allocate the number of taps to be optimum in response to each burst signal input, see column 3, lines 12-20. The equalizer in figure 4 performs equalization in time domain. The reason is the received signal is not transformed into frequency domain. In light of the foregoing disclosure, the equalizer as taught by Uesugi et al. performs similar function as the claimed time domain equalizer (TEQ).

Liu et al. TEQ differs with Uesugi et al. equalizer in that Liu et al. TEQ uses all the taps while Uesugi et al. equalizer allocate or adjust the number of taps to be

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optimum for each signal input without impairing the effect of compensation of waveform distortion due to ISI. Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Liu et al. DMT transceiver can be modified to replace the TEQ 832 with the equalizer as taught by Uesugi et al.. The modification is obvious because of the following reasons: both equalizers are utilized in a receiver to reduce intersymbol interference; Uesugi et al. equalizer use less than the total number of taps in response to an input signal, thereby reducing the number of required arithmetic and logic processing operations, and attaining the desired reduction of the power consumption and size of the equalizer. With the modification, the equalizer as taught by Uesugi et al. allocates the number of taps to be optimum for each Nyquist rate sequence disclosed in Liu et al. teachings.

Regarding claim 2, Liu et al. does not expressly teach the Discrete Fourier Transform (DFT) 833 for adjusting the demodulation rate as set forth in the claim.

In column 24 line 35 through column 25 line 35, Liu et al. teaches a method for determining an optimum sampling rate by dividing the over-sampled sequence into N separate Nyquist rate sequences. Then, the shortened channel impulse response for each of N separate Nyquist rate sequences is measured and the Nyquist rate sequence providing the best performance is selected. In light of the foregoing teachings, it would have been obvious for one of ordinary skill in the art at the time the invention was made that DFT 833 in figure 8 must accommodate the selected Nyquist rate sequence, which provides the best performance. The motivation is that DFT 833 performs a DFT on the

time-domain symbol on the selected Nyquist rate sequence among N separate Nyquist rate sequences. In view of the foregoing discussion, DFT 833 performs similar function as the claimed means for adjusting a demodulation rate.

Regarding claim 3, as recited in claim 1, referring to figure 20, in column 24 lines 35-67, the digital filter 2006 filters the over-sampled sequence received from the ADC 2004, and performs a decimation function to provide a sequence of samples to the TEQ. Liu et al. further teaches that the digital filter may output every Nth filtered sample to the TEQ 832. The over-sampled sequence includes N separate Nyquist rate sequences, each consisting of every Nth filtered sample starting from different delay within the over-sampled sequence. In view of the foregoing discussion, the digital filter 2006 performs function as a decimator to output variable Nyquist rate sequences to the TEQ 832. Hence, the digital filter 2006 corresponds to the claimed decimator.

Regarding claim 4, referring to figure 7 of Uesugi et al. invention, the equalizer 34 includes:

- a delay line comprising a plurality of delay elements 2 accepting successive portions of the received communication channel as claimed, see column 3, lines 45-60;

- taps off of the successive portions of the delay line with each tap configured to scale each successive portion by an associated weighting element 3 to provide a corresponding scaled output as claimed, see column 3, lines 45-60;

- a summer 4 coupled to the taps to sum the scaled outputs as claimed;

and a switch controller 43 controls the position of each of the selector switches 7a to 7e in the equalizer according to the result of the tap allocation determined by the tap allocation determiner; see column 6, lines 20-55. In view of the foregoing discussion, the switch controller 43 varies the number of taps to be optimum for each input signal, and corresponds to the claimed controller.

Regarding claim 5, referring to figure 7 of Uesugi et al. invention again, the delay line as recited in claim 4 further includes:

- a plurality of delay elements 2 corresponding to the claimed delay buffers;
- a plurality selector switches 7a to 7e serially coupling delay elements 2 one to another to form a delay line accepting successive portions of the received communication channel, and selector switches 7a and 7e is controlled by the switch controller 43, which allocates a number of taps (e.g. uncoupling one or more delay elements 2) to be optimum for an signal input, thereby shortening the length of the delay line. In view of that, selector switches 7a to 7e correspond to the claimed switches

Regarding claim 10, as recited in claim 1, in Liu et al. invention, figure 7 illustrates an exemplary ADSL modem including a DMT transceiver 704 as shown in figure 8. The DMT transceiver in figure 8 includes a transmit and a receive path, and is coupled to the subscriber loop 705 via the hybrid 820. Hence, the ADSL modem in figure 7 corresponds to the claimed modem.

Liu et al. does not teach a time domain equalizer (TEQ) as set forth in the claim.

Uesugi et al. discloses an equalizer for use in a data receiver, in which the number of required taps can be reduced without impairing the effect of compensation of waveform distortion due to the components appearing after the main waveform component relative to time and that due to the components appearing before the main waveform component relative to time; see column 2, lines 46-67. The aforementioned phenomenon is called intersymbol interference as well known in the art of communications. Figure 4 illustrates an embodiment of the equalizer including a plurality of delay elements 2, a plurality of weighting elements 3 applied to an adder 4, a plurality of selector switches 7a to 7e disposed in line with the respective delay elements 2; see column 3, lines 45-67. In operation, the selector switches disposed in line with the delay lines of the equalizer are utilized to allocate the number of taps to be optimum in response to each burst signal input, see column 3, lines 12-20. The equalizer in figure 4 performs equalization in time domain. The reason is the received signal is not transformed into frequency domain. In light of the foregoing disclosure, the equalizer as taught by Uesugi et al. performs similar function as the claimed time domain equalizer (TEQ).

Liu et al. TEQ differs with Uesugi et al. equalizer in that Liu et al. TEQ uses all the taps while Uesugi et al. equalizer allocate or adjust the number of taps to be optimum for each signal input without impairing the effect of compensation of waveform distortion due to ISI. Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Liu et al. DMT transceiver can be modified to replace the TEQ 832 with the equalizer as taught by Uesugi et al.. The

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modification is obvious because of the following reasons: both equalizers are utilized in a receiver to reduce intersymbol interference; Uesugi et al. equalizer use less than the total number of taps in response to an input signal, thereby reducing the number of required arithmetic and logic processing operations, and attaining the desired reduction of the power consumption and size of the equalizer.

Regarding claim 12, claim 12 is rejected on the same ground as for claim 4 because of similar scope.

Regarding claim 13, claim 13 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 17, the ADSL modem in figure 7 includes a discrete multitone transceiver, which supports discrete multitone modulation and demodulation.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uesugi et al. U.S. Patent 5,563,911.

Regarding claim 18, Uesugi et al. discloses an equalizer for use in a data receiver apparatus. The equalizer operates in time domain to compensate waveform distortion due to ISI, see column 2 lines 45-60. Uesugi et al. does not teach a method for time domain equalization as set forth in the claim. However, Uesugi et al. discloses an equalizer including components similar to those of the claimed invention, therefore, it

would have been obvious for one of ordinary skill in the art at the time the invention was made that the equalizer as taught by Uesugi et al. can perform the claimed steps. The motivation is that the equalizer including similar components with the claimed invention should be able to perform similar steps.

Referring to figure 4, in column 3 lines 45-60, figure 4 illustrates an equalizer including:

a plurality of delay elements 2 for delay buffering successive portions of a received communication channel;

a plurality of weighting elements 3 for scaling each successive portion of the received communication channel buffered in the delay element 2, each output from a weighting element is a scaled output associated with coefficient of the weighting element;

a summer 4 for summing the scaled outputs from the plurality of weighting elements 3;

a plurality of selector switches 7a to 7e disposed in line with the respective delay elements 2 used for allocating the number of taps, the selector switches 7a to 7e performing to the claimed step of varying a number of successive portions of the receive communication channel buffered in delay elements 2.

Allowable Subject Matter

6. Claims 6-7, 11, 14-16, and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 6 and 14, claims 6 and 14 are indicated allowable because Uesugi et al. fails to disclose the claimed limitations "switches as set forth in the claim".

Regarding claims 7 and 15, claims 7 and 15 are indicated allowable because even though Liu et al. discloses a tap allocation determiner 42 as shown in figure 7, tap allocation determiner 42 does not perform as the claimed skip controller as set forth in the claimed invention.

Regarding claim 11, claim 11 is indicated allowable because Liu et al. and Uesugi et al. fail to disclose, "means for determining a highest usable frequency component of the received communication channel" and "the TEQ responsive to a determination of the highest usable frequency as set forth in the claim".

Regarding claim 16, claim 16 is indicated allowable because even though Liu et al. discloses a switch controller 43 as shown in figure 7, switch controller 43 does not "vary the length of the delay line inversely with respect to a length of the at least subscriber line".

Regarding claim 19, claim 19 is indicated allowable because Uesugi et al. fails to teach the claimed step as set forth in the claimed.

Regarding claim 20, claim 20 is indicated allowable because Uesugi et al. fails to teach the claimed limitations "varying a number of successive portions of the received".

communication channel... inversely with respect to the highest usable frequency of the received communication channel determined in the determining act".

7. Claim 8 is allowed.

Regarding claim 8, claim is allowable over the prior art of record since the cited references taken individually or in combination fails to disclose a method for suppressing ISI in a received communication channel of a modem comprising the step of "adjusting at least one of a number of time domain equalization taps operating on the receive path responsive to the adjustment of the sampling rate in the act of adjusting the sampling rate", which is performed after the step of "determining a highest useful frequency component" as set forth in the claim, and the step of "adjusting the sampling rate of the received communication channel" as set forth in the claim. It is noted that the closest prior art, Liu et al. (US Patent 6,754,261 B1) and Uesugi et al. (US Patent 5,563,911) shows a similar method for determining optimal sampling time. However, Liu et al. and Uesugi et al. disclose the step of "determining a highest useful frequency component" as set forth in the claim and the step of "adjusting the sampling rate of the received communication channel" as set forth in the claim, but fail to disclose the step of "adjusting at least one of a number of time domain equalization taps operating on the receive path responsive to the adjustment of the sampling rate in the act of adjusting the sampling rate".

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tanaka et al. U.S. Patent 5,274,512 discloses "Coefficient Control System For Digital Equalizer Using Orthogonal Oscillation".

Liu et al. U.S. Patent 6,674,795 B1 discloses "System, Device And Method For Time-Domain Equalizer Training Using An Auto-Regressive Moving Average Model".

Uesugi et al. U.S. Patent 5,388,123 discloses "Data Receiving System".

Harikumar et al. U.S. Patent 6,631,175 B2 discloses "Spectrally Constrained Impulse Shortening Filter For A Discrete Multi-Tone Receiver.

Uesugi et al. U.S. Patent 5,444,739 discloses "Equalizer For Data Receiver Apparatus".

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran

11/26/2004

KHANH TRAN